REMARKS/DISCUSSION OF ISSUES

By this Amendment, Applicants cancel claim 14 without disclaimer of the underlying subject matter or prejudice against future prosecution. Applicants also amend claims 1, 4, 5, 8, 11-12, 15, 19 and 22, and add new claims 23-27. Support for the new and amended claims can be found throughout the specification and drawings, and specifically in paragraphs [0039], [0040], [0046], and [0055] – [0060]; Tables 3, 6 & 7; and FIGs. 4B & 7. Accordingly, claims 1, 2, 4-9, 11-13, 15-16, 18-20, and 22-27 remain pending in the application.

Reexamination and reconsideration are respectfully requested in view of the following Remarks.

35 U.S.C. § 101

The Office Action rejects claims 1, 2, 4-9, 11-13, 15-16, 18-20, and 22 under 35 U.S.C. § 101 as supposedly being directed to non-statutory subject matter.

Applicants respectfully traverse these rejections for at least the following reasons.

Claims 1 and 22

The Office Action cites the specification at paragraph [007] for the proposition that claims 1 and 22 are directed toward "software *per se*."

Applicants respectfully disagree.

Paragraph [0007] says that a receiver "*may be implemented in hardware, as well as software (i.e., digital signal processor embodiment)*."[1] Properly understood, the text discloses that the receiver may be implemented – among other ways – with a processor *("i.e., a digital signal processor")* executing software. "Software" standing alone, and absent a processor, cannot perform any functions, and Applicants respectfully submit that nothing in the specification discloses otherwise.

Meanwhile, claim 1 clearly recites, *inter alia*, "*a first processing block capable*

1 Please note also that the specification in paragraph [0007] uses the words "hardware as well as software" as opposed to, for example, "hardware ***OR*** software." The phrase "*as well as*" can be interpreted to mean "*and in addition*" (see, e.g., http://www.answers.com/topic/as-well-as) or "*including; in addition to*" (see, e.g., http://esl.about.com/library/glossary/bldef_a_20.htm).

of receiving a dual bitstream signal." "Pure" software being nothing more than a set of executable instructions cannot receive a dual bitstream signal. However, e.g., a digital signal processor operating in conjunction with software can receive a dual bitstream signal.

Similarly, claim 22 clearly recites, *inter alia*, a standard de-randomizer capable of de-randomizing bytes associated with a standard stream. "Pure" software being nothing more than a set of executable instructions is not capable of de-randomizing bytes associated with a standard stream. However, e.g., a digital signal processor operating in conjunction with software can de-randomize bytes associated with a standard stream.

Therefore, Applicants respectfully submit that the specification does not disclose that claims 1 and 22 are directed towards software *per se*, and indeed Applicants respectfully submit that claims 1 and 22 are not directed toward software *per se*. Furthermore, Applicants respectfully submit that claims 1 and 22 are directed towards statutory subject matter under 35 U.S.C. § 101.

Claim 8

Claim 8 is specifically directed to ***a method*** comprising a plurality of recited steps.

Applicants respectfully submit that, while the method, at least in part, may be ***performed by*** a processor executing software, the recited method is not, and cannot be, "software *per se*."

Therefore, Applicants respectfully submit that the specification does not disclose that claim 8 is directed towards software *per se*, and indeed Applicants respectfully submit that claim 8 is not directed toward software *per se*. Furthermore, Applicants respectfully submit that claim 8 is directed towards statutory subject matter under 35 U.S.C. § 101.

Claim 15

The Office Action states that independent claim 15 depends from claim 1, 8 or 22 (see Office Action at page 3, lines 1-2).

Applicants respectfully disagree.

Claim 15 is an independent claim and does not depend from any other claim. Furthermore, among other things, claim 15 recites "*receiver front-end* ***circuitry*** *capable of receiving and down-converting a dual bitstream signal*" (emphasis added).

Applicants respectfully submit that circuitry cannot be "software *per se*."

Accordingly, Applicants respectfully submit that claim 15 is directed towards statutory subject matter under 35 U.S.C. § 101.

Claims 2, 4-7, 9, 11-13, 16, 18-20 depend variously from the afore-mentioned claims 1, 8, 22 and 15 and Applicants respectfully submit that the rejections thereof under 35 U.S.C. § 101 are improper for the reasons set forth above.

Accordingly, for at least these reasons, Applicants respectfully submit that claims 1, 2, 4-9, 11-13, 15-16, 18-20, and 22 are all patentable under 35 U.S.C. § 101. Therefore, Applicants respectfully request that the rejections of claims 1, 2, 4-9, 11-13, 15-16, 18-20, and 22 are all patentable under 35 U.S.C. § 101 all be withdrawn.

35 U.S.C. § 103

The Office Action rejects claims 1, 4-5, 7-8, 11-12, 15 and 18-19 under 35 U.S.C. § 103 over Strolle et al. U.S. Patent Application Publication 2004/0028076 ("Strolle") in view of Limberg U.S. Patent Application Publication 2004/0237024 ("Limberg I"); claims 2, 9 and 16 under 35 U.S.C. § 103 over Strolle in view of Limberg I and further in view of Hurst, Jr. U.S. Patent 6,034,731 ("Hurst"); claims 6, 13 and 20 under 35 U.S.C. § 103 over Strolle in view of Limberg I and further in view of Fimoff U.S. Patent Application Publication 2001/0055342 ("Fimoff"); and claim 22 under 35 U.S.C. § 103 over Strolle in view of Limberg U.S. Patent 6,621,527 ("Limberg II").

Applicants respectfully submit that all of the claims are patentable over the cited art for at least the following reasons.

Claim 1

Among other things, the packet formatter of claim 1 includes a second processing block capable of determining the locations of the parity bytes within each

robust packet according to the robust packet's position within the frame, in response to which the first processing block removes the header bytes and parity bytes from the dual bitstream signal to output a first output signal.

Applicants respectfully submit that no combination of the cited references would ever produce a packet formatter including this combination of features.

Strolle discloses a bitstream that includes normal packets and robust packets. Strolle also discloses that when a standard Reed-Solomon encoder is employed to generate the normal packets, then the parity bytes are output at the end of the decoded normal packets generated by a corresponding Reed-Solomon encoder. Strolle also discloses that when a non-standard Reed-Solomon encoder is employed to generate the robust packets, then the parity bytes in the robust packets are relocated so that the parity bytes all come out of the corresponding non-standard Reed-Solomon decoder first for the decoded robust packets. See paragraphs [0061]-[0063].

Strolle also discloses that the locations of the robust packets and the normal packets within a frame are known by reference to a robust mode tier control code value which is communicated to the receiver. See paragraph [0049].

Strolle further discloses that, at the receiver, the non-standard Reed-Solomon decoder must reorder the bytes for each packet depending on whether it is a robust packet or a normal packet, which can be determined from where the packet is located in the frame (using the robust mode tier control code value). See paragraphs [0083]-[0084].

It is evident from the above description that in Strolle the locations of the parity bytes in the robust packets are different than the locations of the parity bytes in the normal packets. However, the locations of the parity bytes in all of the robust packets are the same as each other so that the parity bytes for each robust packet always come out of the non-standard Reed-Solomon decoder first.

Therefore, Applicants respectfully submit that Strolle does not disclose a second processor block capable of determining the locations of the parity bytes within each robust packet **according to the robust packet's position within the frame**.

Indeed, as explained above, Applicants respectfully submit that Strolle teaches that the locations of the parity bytes within each robust packet are the same as each other **regardless of the robust packet's position within the frame**.

Therefore Applicants respectfully submit that no combination of Strolle and Limberg I would produce the packet formatter of claim 1.

Also among other things, the packet formatter of claim 1 includes a third processing block capable of receiving a first output signal and removing therefrom duplicate bits associated with the robust stream to thereby produce a second output signal that is output from a data path output of the packet formatter.

The Office Action fairly admits that Strolle does not disclose the recited third processing block. However the Office Action states that Limberg I discloses a third processing block including these features, and proposes to modify Strolle's system to include the third processing block of claim 1.

Applicants traverse the proposed combination of Strolle and Limberg I for at least the following reasons.

At the outset, Applicants respectfully submit that the Office Action fails to establish the level of ordinary skill in the art of invention of claim 1. This is a fundamental requirement for maintaining a rejection under 35 U.S.C. § 103. See M.P.E.P. §§ 2141(II)(C) and 2141.03. Thus the Office Action fails to perform the analysis required by KSR International Co. v. Teleflex Inc., 550 U.S. 398, 82 USPQ2d 1385 (2007) ("KSR") for rejecting a claim under 35 U.S.C. § 103.

Furthermore, a rejection on obviousness grounds under 35 U.S.C. § 103 cannot be sustained by mere conclusory statements: instead there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. See M.P.E.P. § 2142 (quoting In re Kahn, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) and KSR 82 USPQ2d at 1396 (2007) (quoting Federal Circuit statement with approval)).

Applicants respectfully submit that the proposed combination of Strolle and Limberg I to attempt to construct the method of claim 1 is not based on an articulated reasoning with any rational underpinnings, but instead is based on conclusory

statements which lack reason.

The Office Action states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Strolle to add a third processing block capable of receiving the first output signal and removing therefrom duplicate bits associated with the robust stream to thereby produce a second output signal that is output from a data path output of the packet formatter, "*in order to remove error correction bits (redundant bits) performed* (sic) *by the Forward Error Correction Coders*."

However, Applicants respectfully submit that Strolle's transmit system does not transmit a signal where each packet includes such duplicate bits ("redundant bits"). So modifying Strolle to add a third processing block capable of receiving the first output signal and removing therefrom duplicate bits associated with the robust stream to thereby produce a second output signal that is output from a data path output of the packet formatter to Strolle, would not "*remove error correction bits (redundant bits)*" – because no such bits exist to be removed! Indeed, all that the proposed modification would do is to turn Strolle's receiver into a non-functional device that would output incorrect data. Thus Applicants respectfully submit that there is no reason for the proposed combination, and that the proposed combination is improper.

Therefore, for at least these reasons, Applicants respectfully submit that claim 1 is patentable over the cited art. Accordingly, Applicants respectfully request that the rejection of claim 1 be withdrawn and that claim 1 be allowed.

Claim 8

Among other things, the method of claim 8 includes: determining the locations of the parity bytes within a robust packet according to the robust packet's position within its frame; and removing from a first output signal duplicate bits associated with a robust stream to thereby produce a second output signal that is output from a data path output of a packet formatter.

As explained above with respect to claim 1, Applicants respectfully submit that the prior art does not teach any method including such a combination of features.

Applicants also respectfully traverse the proposed combination of proposed combination of Strolle and Limberg I for at least the reasons set forth above with respect to claim 1.

Therefore, for at least these reasons, Applicants respectfully submit that claim 8 is patentable over the cited art. Accordingly, Applicants respectfully request that the rejection of claim 8 be withdrawn and that claim 8 be allowed.

Claim 15

Among other things, the receiver of claim 15 includes: (1) a second processing block capable of determining the locations of the parity bytes within the current packet according to the current packet's position within its frame, in response to which a first processing block removes the header bytes and parity bytes from dual bitstream signal to output a first output signal; and (2) a third processing block capable of receiving the first output signal and removing therefrom duplicate bits associated with a robust stream to thereby produce a second output signal that is output from a data path output of a packet formatter.

As explained above with respect to claim 1, Applicants respectfully submit that the prior art does not teach any method including such a combination of features. Applicants also respectfully traverse the proposed combination of proposed combination of Strolle and Limberg I for at least the reasons set forth above with respect to claim 1.

Therefore, for at least these reasons, Applicants respectfully submit that claim 15 is patentable over the cited art. Accordingly, Applicants respectfully request that the rejection of claim 15 be withdrawn and that claim 15 be allowed.

Claims 2, 4-7, 9, 11-13, 16, 18-20

Claims 2, 4-7, 9, 11-13, 16, 18-20 depend variously from claims 1, 8 and 15, and are deemed patentable over the cited art for at least the reasons set forth above with respect to claims 1, 8 and 15, and for the following additional reasons.

Among other things, in the packet formatter of claim 5, and the receiver of claim 19, the second processing block includes a look-up table which identifies the locations of the parity bytes for each robust packet depending upon the location of

the robust packet within the frame. In the method of claim 12, the step of determining the locations of the parity bytes comprises the step of determining the locations of the parity bytes from a look-up table which identifies the locations of the parity bytes for each robust packet depending upon the location of the robust packet within the frame.

The Office Action cites paragraph [0079] of Strolle as supposedly disclosing this feature.

Applicants respectfully disagree.

Paragraph [0079] of Strolle discloses that a map is created of which VSB symbols normal and which are robust.

However, Applicants respectfully submit that the cited text does not disclose a look-up table which identifies the locations of the parity bytes for each robust packet depending upon the location of the robust packet within the frame, as recited in claims 5, 12 and 19.

Accordingly, for at least this additional reason, Applicants respectfully submits that claims 5, 12 and 19 are patentable over the cited art.

Claims 2, 9 and 16

Claims 2, 9 and 16 depend variously from claims 1, 8 and 15. Applicants respectfully submit that Hurst does not remedy the defects of Strolle and Limberg I as set forth above with respect to claims 1, 8 and 15. Therefore claims 2, 9 and 16 are deemed patentable over the cited art for at least the reasons set forth above with respect to claims 1, 8 and 15, and for the following additional reasons.

Claims 2, 9 and 16 all include a feature of passing bytes associated with the standard stream to the data path output of the packet formatter after delaying the standard stream bytes by a predetermined delay time.

The Office Action states that Hurst teaches this feature.

Applicants respectfully disagree.

Hurst teaches that an MPEG picture header contains a delay number that indicates that indicates the mount of time that a video decoder should wait after the picture header enters the decoder's video buffer before decoding the picture.

Hurst does not teach passing bytes associated with the standard stream to the data path output of a packet formatter after delaying the standard stream bytes by a predetermined delay time. So no combination of Hurst with Strolle and Limberg I teaches the subject matter of claims 2, 9 and 16.

Applicants also respectfully traverse the proposed combination of Hurst with Strolle and Limberg I as lacking any reason therefor.

Applicants respectfully submit that the proposed combination would not synchronize audio and video packets. The elements in Strolle cited in the Office Action as supposedly corresponding to the recited packet formatter are all operating on **transmission** packets, which will of course include both audio packets and video packets – as well as other packets. Therefore any delay applied to packets by such as packet formatter would be also applied to both audio packets and video packets, and would not perform any the "synchronization" which is proposed as the reason for the modification of Strolle.[2]

Accordingly, for at least this additional reason, Applicants respectfully submits that claims 2, 9 and 16 are patentable over the cited art.

Claims 6, 13 and 20

Claims 6, 13 and 20 depend variously from claims 1, 8 and 15. Applicants respectfully submit that Fimoff does not remedy the defects of Strolle and Limberg I as set forth above with respect to claims 1, 8 and 15. Therefore claims 6, 13 and 20 are deemed patentable over the cited art for at least the reasons set forth above with respect to claims 1, 8 and 15.

Claim 22

Among other things, the data re-randomizer of claim 22 includes a robust de-randomizer and a delay calculation circuit for applying a control signal to the robust de-randomizer to cause the robust de-randomizer to suspend its operation for a

2 Also note, for example, that in claim 19 the second processing block is clearly recited as preceding even the Reed Solomon decoder. Thus the second processing block which delays the standard stream bytes by a predetermined delay time, operates on packets before they are ever decoded and demultiplexed into video and audio packets, and before video packets could be reassembled into video frames and presented to a video decoder.

portion of a field in accordance with a determined delay.

Applicants respectfully submit that the cited art does not disclose or suggest a data re-randomizer that includes this feature.

Therefore, for at least these reasons, Applicants respectfully submit that claim 22 is patentable over the cited art. Accordingly, Applicants respectfully request that the rejection of claim 22 be withdrawn and that claim 22 be allowed.

NEW CLAIMS 23-27

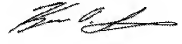
New claims 23-27 depend variously from claims 1, 8, 15 and 22 and are deemed patentable over the cited art for at least the reasons set forth above with respect to claims 1, 8, 15 and 22, and for the various novel features recited therein.

CONCLUSION

In view of the foregoing explanations, Applicants respectfully request that the Examiner reconsider and reexamine the present application, allow claims 1, 2, 4-9, 11-13, 15-16, 18-20, and 22-27, and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283.0720 to discuss these matters. Correspondence should be addressed to the correspondence address of record at the USPTO.

Respectfully submitted,

VOLENTINE & WHITT



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